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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

AR

Office Action Summary	Application No.	Applicant(s)	
	10/776,016	CHANG, DONG-SOO	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/10/04, 6/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS 1/27/05*.

DETAILED ACTION

Claim Objections

Claim 7 is objected to because of the following informalities:

Line 20 should begin "The method of fabricating the CMOSFET of claim 1...." Appropriate correction is required.

Claims 21-30 are objected to because of the following informalities:

Line 7 in claim 21 recites a "second lightly doped region," but no first lightly doped region is claimed. Additionally, line 12 recites a "third heavily doped region," but no second heavily doped region is claimed. Finally, line 15 recites a "fourth lightly doped region," but no second or third lightly doped regions are claimed. However, if applicant changes claim 21 to recite in line 7 a "first lightly doped region," in line 12 a "second heavily doped region," and in line 15 a "second heavily doped region," it appears to the examiner that claim 21 will be identical to claim 9. Claims 22-30 are objected to for depending from claim 21. Appropriate correction is required.

Claim 26 is objected to because of the following informalities:

In lines 5 and 9, the word "doped" should be inserted between "heavily" and "region." In lines 7 and 11, the word "doped" should be inserted between "lightly" and "region." Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 3-6, 9-16, 21-24, and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Grider et al. (U.S. 6,632,718).

Regarding claim 1, Grider et al. teaches a method of fabricating a CMOSFET comprising forming a plurality of gate patterns on a first region (**120** in Fig. 1C) and a second region of a semiconductor substrate (**122** in Fig. 1C; Grider et al. claim 1); then forming gate spacers on both sidewalls of the gate patterns (**114** in Fig. 1C); forming a first impurity region of a first conductivity type in the first region of the semiconductor substrate (**124** in Fig. 1D; column 3, lines 12-19); then removing the gate spacers exposed at the first region (Fig. 1E; column 3, lines 20-22); then forming a second impurity region from which the gate spacers have been removed, the second impurity region having shallower depth than the first impurity region (**126** in Fig. 1E; column 3, lines 23-26); then forming a third impurity region of a second conductivity type in the second region (**134** in Fig. 1F; column 3, lines 54-58); then removing the gate spacers exposed at the second region (Fig. 1G; column 3, lines 59-61); and then forming a fourth impurity region of the second conductivity type in the second region, the fourth

impurity region having shallower depth than the third impurity region (**136** in Fig. 1G; column 3, lines 62-65).

Regarding claim 2, Grider et al. teaches the method of fabricating the CMOSFET of claim 1, and further teaches that the first impurity region has higher impurity concentration than the second impurity region, and the third impurity region has higher impurity concentration than the fourth impurity concentrations (column 2, lines 19-27—the first and third impurity regions are source/drain implants while the second and third impurity regions are *lightly-doped* source/drain implants, which by definition have lower impurity concentrations.)

Regarding claim 4, Grider et al. teaches the method of fabricating the CMOSFET of claim 1, and further teaches that the first impurity region is formed in the first region, using the gate pattern and the gate spacers as an ion implantation mask (**124** in Fig. 1D; column 3, lines 12-19); the second impurity region is formed in the first region, using the gate pattern as an ion implantation mask (**126** in Fig. 1E; column 3, lines 23-26); the third impurity region is formed in the second region, using the gate pattern and the gate spacers as an ion implantation mask (**134** in Fig. 1F; column 3, lines 54-58); and the fourth region is formed in the second region, using the gate pattern as an ion implantation mask (**136** in Fig. 1G; column 3, lines 62-65).

Regarding claim 5, Grider et al. teaches the method of fabricating the CMOSFET of claim 1, and further teaches that the gate spacers comprise silicon (SiGe, column 2, lines 52-61).

Regarding claim 6, Grider et al. teaches the method of fabricating the CMOSFET of claim 1, and further teaches that removing the gate spacers at the first region and second region is performed by isotropic etching (column 3, lines 20-22 and 59-61).

Regarding claims 9 and 21, Grider et al. teaches a method of fabricating a CMOSFET comprising the steps of forming a plurality of gate patterns on a first region (**120** in Fig. 1C) and a second region of a semiconductor substrate (**122** in Fig. 1C; Grider et al. claim 1); then forming gate spacers on both sidewalls of the gate patterns (**114** in Fig. 1C); then forming a first mask, which covers the second region and exposes the first region (**116** in Fig. 1D); then forming a first heavily doped region of a first conductivity type in the first region (**124** in Fig. 1D; column 3, lines 12-19); then removing the gate spacers exposed at the first region (Fig. 1E; column 3, lines 20-22); then forming a first lightly doped region of the first conductivity type in the first region (**126** in Fig. 1E; column 3, lines 23-26; column 2, lines 22-26 indicates the source/drain extensions can be moderately or lightly doped); then removing the first mask (column 3, lines 39-40); then forming a second mask which covers the first region and exposes the second region (**130** in Fig. 1F); then forming a second heavily doped region of a second conductivity type in the second region (**134** in Fig. 1F; column 3, lines 54-58); then removing the gate spacers exposed at the second region (Fig. 1G; column 3, lines 59-61); and then forming a second lightly doped region of the second conductivity type in the second region (**136** in Fig. 1G; column 3, lines 62-65; column 2, lines 22-26 indicates the source/drain extensions can be moderately or lightly doped); and then removing the second mask (column 3, lines 66-67; Fig. 1H).

Regarding claims 10, 11, 22, and 23, Grider et al. teaches the method of fabricating the CMOSFET of claims 9 and 21, and further teaches that the first conductivity type is n type (column 3, lines 12-19) and the second conductivity type is p type (column 3, lines 54-58).

Regarding claims 12, 13, and 26, Grider et al. teaches the method of fabricating the CMOSFET of claims 9 and 21, and further teaches that the forming of the first heavily doped region includes an ion implantation process which uses the first mask, the gate pattern, and the gate spacer of the first region as an ion implantation mask (Fig. 1D); and the forming of the first lightly doped region includes an ion implantation process which uses the first mask and the gate pattern of the first region as an ion implantation mask (Fig. 1E); and the forming of the second heavily doped region includes an ion implantation process which uses the second mask, the gate pattern and gate spacer of the second region as an implantation mask (Fig. 1F); and the forming of the second lightly doped region includes an ion implantation process which uses the second mask and gate pattern of the second region as an ion implantation mask (Fig. 1G).

Regarding claims 14 and 24, Grider et al. teaches the method of fabricating the CMOSFET of claims 9 and 21, and further teaches that the first lightly doped region has shallower depth than the first heavily doped region and the second lightly doped region has shallower depth than the second heavily doped region (Fig. 1H).

Regarding claim 15, Grider et al. teaches the method of fabricating the CMOSFET of claim 9, and further teaches that the gate spacers comprise silicon (SiGe, column 2, lines 52-61).

Regarding claim 16, Grider et al. teaches the method of fabricating the CMOSFET of claim 9, and further teaches that the first and second masks are photoresist patterns which are formed using a photolithographic process (column 2, lines 62-65; column 3, lines 46-49).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 8, 17-20, and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grider et al. (U.S. 6,632,718) in view of Chen et al. (U.S. 2002/0001910).

Regarding claims 7, 8, 17, 19, 27, and 29, Grider et al. teaches the method of fabricating the CMOSFET of claims 1, 9, and 21 (note 35 U.S.C. 103(e) rejection above), but does not teach before forming the third impurity region, forming a first HALO ion implantation to form a first HALO region, wherein the first HALO region is formed to cover sides of the first impurity region beneath the second impurity region, or after forming the fourth impurity region, performing a second HALO ion implantation to form a second HALO region, wherein the second HALO region is formed to cover sides of the

third impurity region beneath the fourth impurity region. Grider et al. also does not teach that the first HALO ion implantation process uses the gate pattern of the first region and the first mask as an ion implantation mask (instant claims 17 and 27) or that the second HALO ion implantation process uses the gate pattern of the second region and the second mask as an ion implantation mask (instant claims 19 and 29).

Chen et al. teaches a method of fabricating a MOSFET that involves ion-implanting source/drain regions (**48** and **50** in Fig. 5) using spacers (**46** in Fig. 5) to mask the implantation, removing the spacers (Fig. 6), and performing a second, shallow ion implantation (**52** in Fig. 6), and then performing a HALO ion implantation (**96** in Fig. 6), using the gate pattern of the MOSFET region as an ion-implantation mask, wherein the HALO region is formed to cover the sides of the source/drain regions (Fig. 6). Chen et al. teaches that the purpose of the HALO implantation is to inhibit the occurrence of abnormal punch-through between the source and drain (paragraphs 0035-0036).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Grider et al. and Chen et al. by fabricating MOSFET gates with spacers in two regions of a semiconductor substrate, mask one of the regions with photoresist, form deep impurity regions in the first region of the semiconductor, remove the spacers, and form shallow impurity regions in the first region of the semiconductor as taught by Grider et al., and then perform HALO implantations to cover the sides of the deep implant regions beneath the shallow implant regions using the gate pattern of the first-region MOSFET as an implantation mask, as taught by Chen et al. Grider et al. teaches that the second semiconductor

region is covered in a photoresist layer, so the HALO implantation would necessarily also use that photoresist layer as a mask. It would then be obvious to continue with the method as taught by Grider et al. and mask the first semiconductor region and repeat the process in the second semiconductor region, again inserting the HALO implantation step, as taught by Chen et al. after the last shallow implantation step, since Chen does not limit this method to a particular type of MOSFET (paragraph 0035).

The motivation for doing so at the time of the invention would have been to minimize the occurrence of abnormal punch-through between the source and drain of the individual MOSFETs, as expressly taught by Chen et al.

Regarding claims 18, 20, 28, and 30, Grider et al. and Chen et al. together teach the methods of claims 17, 19, 27, and 29. Chen et al. further teaches that the HALO implantation process is performed by implanting dopants of the same electrical polarity as the semiconductor substrate beneath the source and drain, which decreases the concentration of the PN junction between the bottom of the source/drain regions and the semiconductor beneath them (paragraphs 0035-0036). That means that the source/drain dopants have the opposite electrical polarity as the semiconductor beneath them, and therefore also the opposite electrical polarity as the HALO implants. So at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine Chen et al. with Grider et al. as above, and additionally, in the first HALO ion implantation process use the impurities of the second conductivity type, p-type, (instant claims 18 and 28) and in the second HALO ion implantation process use impurities of the first conductivity type, n-type (instant claims 20 and 30).

The motivation for doing so at the time of the invention would have been to decrease the concentration of the PN junction between the bottom of the source/drain regions and the semiconductor beneath them and also decrease the PN junction capacitance, thus increasing device speed (paragraphs 0035-0036).

Claims 3 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grider et al. (U.S. 6,632,718) in view of Wolf et al. (*Silicon Processing for the VLSI Era*, vol. 1, second edition, 2000).

Regarding claims 3 and 25, Grider et al. teaches the method of fabricating the CMOSFET of claims 1 and 21 and that the first impurity region has higher impurity concentration that the second impurity region, but does not teach that the fourth impurity region has impurity concentration as high as the third impurity region.

Wolf et al. teaches that in a deep submicron FET, the doping level of a source/drain extension (corresponding to the second and fourth impurity regions) can be as high as the source/drain impurity concentration (corresponding to the first and third impurity regions) ($1x10^{15}$ cm^{-2}, pg. 834, lines 4-7 and third full paragraph).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method of fabricating the CMOSFET of claims 1 and 21, as taught by Grider et al., and further fabricate the CMOSFET so that the fourth impurity region has impurity concentration as high as the third impurity region, as taught by Wolf et al.

The motivation for doing so at the time of the invention would have been to fabricate a deep submicron FET, using ion implantation to form the source/drain extensions, as expressly taught by Wolf et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

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